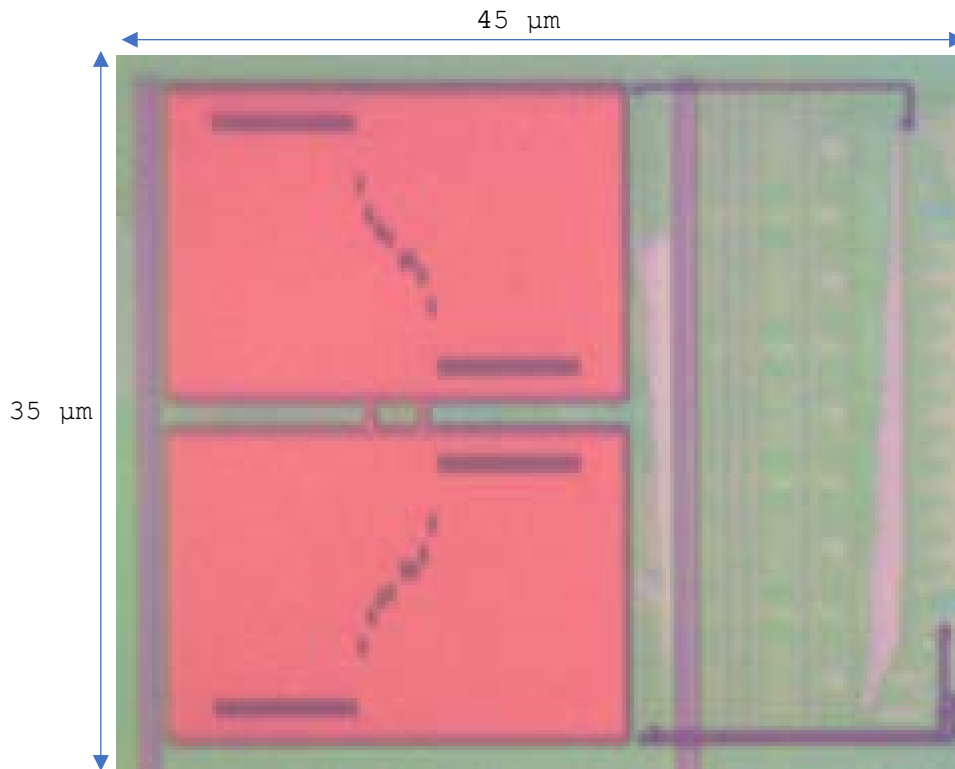# Highly energy-area efficient SAR ADC architecture

45 µm

35 µm

The combination of a unit-length capacitor array and constant common-mode switching provides state-of-the-art energy-area efficiency in analog to digital conversion.

Description

The increasing use of on-chip smart elements such as machine learning tasks or closed-loop control necessitates a larger digital area and power overhead, leaving the analog front-end circuitry with even more demanding constraints. Especially multichannel scenarios in applications ranging from biomedical diagnostic equipment to industrial sensor arrays seek the lowest energy and area per unit channel to increase integration density.

This invention provides an ultra-small (35 µm x 45 µm in 65 nm CMOS) and low-power (50 nW @ 20 kS/s) 10-bit successive approximation register analog-to-digital converter (SAR ADC) architecture, having up to 1 MS/s sampling rate. Applications with stringent area and power constraints, such as multichannel sensors and digital intensive system-on-chips, could benefit from this invention.

Advantages

The footprint of the circuit is very small thanks to realizing binary weights using unit length capacitors, and the energy efficiency is maximized by using the monotonic switching scheme for better charge preservation, while keeping noise performance high using the constant common mode technique.

Moreover, the architecture is highly modular and enables massively parallel sensors within tight power and area constraints.

Applications

- Multi-channel sensor arrays
- Neural implants
- Time-interleaved high-speed ADCs