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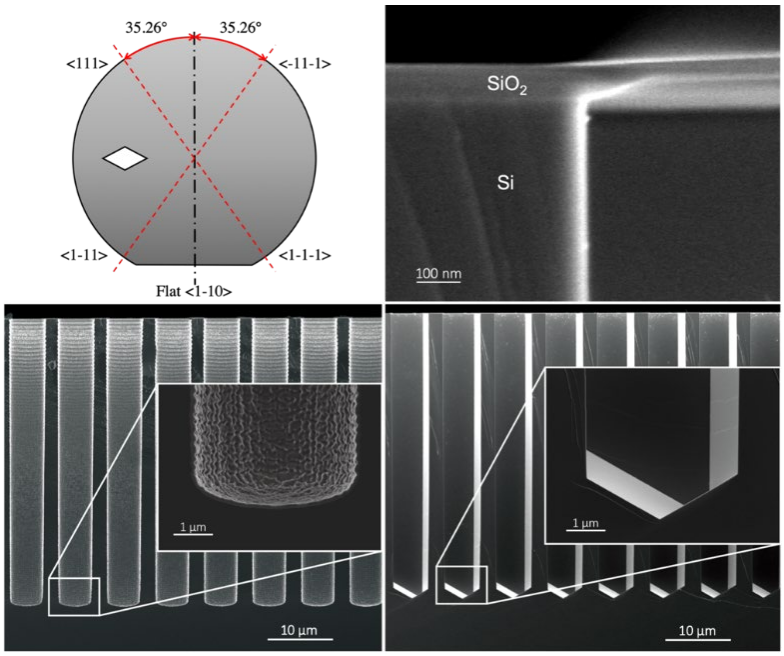
Licensing Opportunity

TTO – Technology Transfer Office

# Fabrication method to remove scalloping and tapering effects in through-silicon vias




Effects of the Michelangelo Process on 5 µm wide, 40 µm deep through silicon vias. It appears evident that wall roughness is completely eliminated, as the effect of tapering along the depth of the via.

Ref. Nr

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Keywords

3D chip integration, Though-silicon vias, silicon fabrication, deep reactive etching, anisotropic etching.

Intellectual Property

Fabrication process step

Publications

S. Frasca *et al.*, "The Michelangelo step: removing scalloping and tapering effects in high aspect ratio through silicon vias", *Scientific Reports* **11**, 3997 (2021)

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## Description

In the last 70 years, the continuous downscaling of semiconductor devices has offered increased device speed and density increases following Moore's prediction. However, as feature sizes got smaller, down to the current 7 nm (i.e. Intel, Samsung, TSMC), there is a physical limitation in scaling before entering the realm of quantum effects. The semiconductor community has shifted towards 3D integration to achieve higher electrical component density and increased performance.

In this context, TSVs are among major technology players in modern high-volume manufacturing. However, the usual standardized TSV fabrication process has to deal with scalloping, an imperfection in the sidewalls caused by the deep reactive ion etching (DRIE). The presence of scalloping causes stress and field concentration in the dielectric barrier, thereby dramatically impacting the following TSV filling step, which is performed by means of electrochemical plating.

We propose here a new scallop free and non-tapered approach to overcome this challenge by adding a new step to the standard TSV procedure exploiting the crystalline orientation of silicon wafers.

## Advantages

Avoiding field concentration and allowing higher aspect ratio is a key aim for TSV fabrication. These aspects require extremely well calibrated processes and expensive machines to damp these effects down. Our approach is a quick and low-cost solution that allows to get better results without the need of such infrastructures.

## Applications

- High quality, high-aspect ratio TSV fabrication for via-first, CMOS 3D integration.
- High quality TSVs for via-last for most non-CMOS fabrication processes.