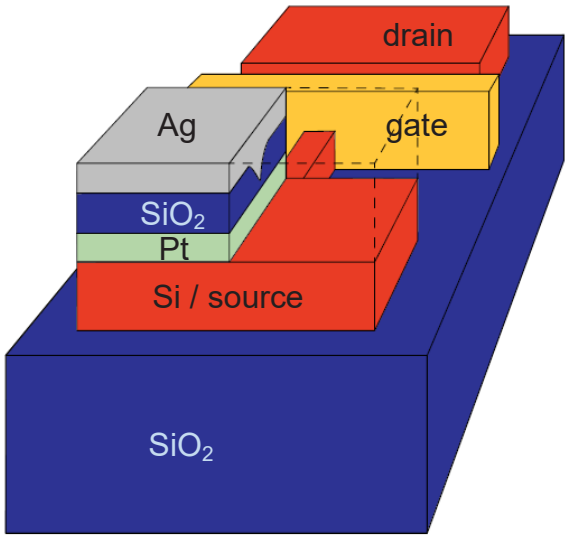
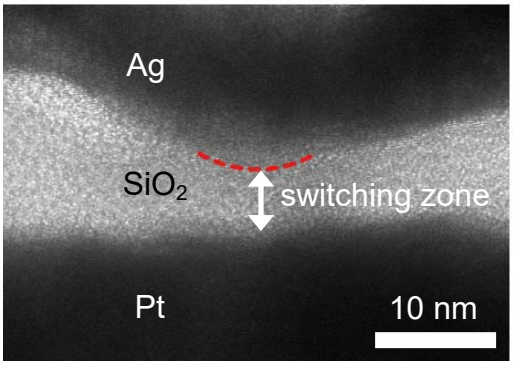
ETH zürich

Licensing Opportunity

Low leakage integrated circuits for Internet-of-Things





(left) Schematic view of the hybrid memristor-transistor technology. The memristor is characterised by an ultra-scaled switching region (20 µm by 20 µm) with a silver 3D tip.

(right) Electron transmission picture of the switching area. Only ten femto Amperes of current leak from the silver to the platinum layer.

Application

A hybrid memristor-transistor technology reduces the power consumption in chip operation by reducing the leakage current. Mobile devices profit by an extended battery lifetime.

Features & Benefits

- reduced power consumption improves battery lifetime
- ideal for low-power and low-frequency applications
- less cost of increased delay and lowered speed
- hysteresis-free and convenient for CMOS integration

Publications

- "Threshold Switching Enabled Sub-pW-Leakage, Hysteresis-Free Circuits", IEEE Transactions on electron devices, 68 (6), 2021 https://doi.org/10.1109/ted.2021.3075393
- Patent pending

Background

Smart mobile devices are typically always-on. Power reduction is key in such devices in order to extend battery lifetime. The leakage power of CMOS circuits has been identified as a significant source of energy dissipation regarding the operation of chips.

Invention

A hybrid memristor-transistor technology is used to reduce the power leakage in chip operation. This invention describes a 3D CBRAM memristor, which is combined with CMOS transistors to build basic logic circuit elements (NOT, NAND, NOR etc.). The memristor connects to the source/drain of a transistor and provides a steep transition between high and low resistance state. This voltage-controlled threshold switch is hysteresis-free and, thus, has a consistent input-output voltage relationship regardless of previous voltage values.

The leakage current is minimized by reducing the area of the switching matrix. Moreover, an electrode with a 3D tip is introduced (see Ag layer in the figure above), which confines the leakage current to the apex of the 3D tip.

Using the suggested hybrid circuit approach, significant power reductions for operation frequencies up to 100 kHz are found. Power reductions in the order of 80% are predicted for 1 kHz operation. This makes the approach ideal for low-power and low-frequency applications.

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Technology Readiness Level