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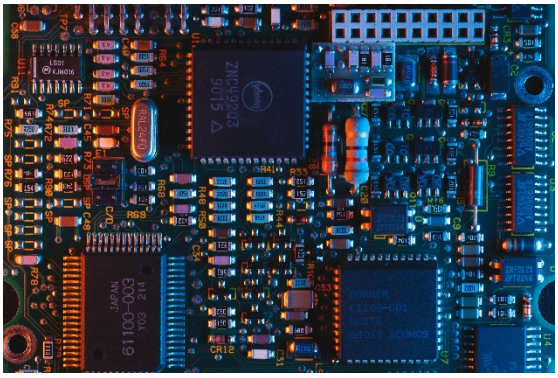
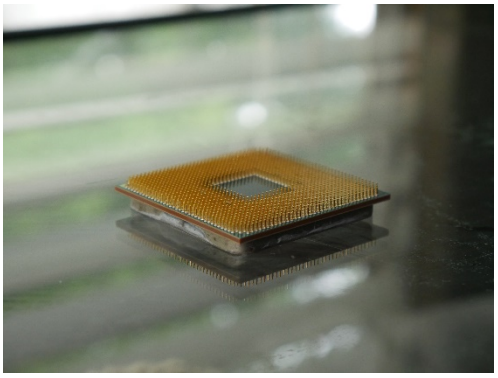
Licensing Opportunity

TTO – Technology Transfer Office

Majority Logic Synthesis





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Keywords

Circuits, optimization, majority logic, Boolean algebra, directed acyclic graphs (DAG), logic synthesis, electronic design automation (EDA)

Intellectual Property

US 10394988 B2

Publications

Amaru et al., "Majority-Inverter Graph: A Novel Data-Structure and Algorithms for Efficient Logic Optimization" in Proceedings of the 51st Design Automation Conference (DAC), 2014

Date

21/07/2020

Description

Electronic Design Automation (EDA) and in particular logic synthesis tools are efficiently representing and optimizing circuits. The performance of modern digital integrated circuits depends directly on the capabilities of these logic synthesis tools. Currently, there are a range of design automation tools which use well-known optimization techniques. In general, they yield good results and are able to handle large circuits as well. As these integrated circuits become more pervasive in various aspects of electronics, there is always a need to further improve the efficacy of logic synthesis. This invention aims to provide a logic synthesis tool which significantly improves the performance of digital integrated circuits in several ways.

This invention offers a novel method to both represent and optimize a logic circuit. It consists of only majority and inversion Boolean operators. A majority operator returns a logic value assumed by more than half of the inputs, whilst inversion returns the inverse of the input. The method uses a Majority-Inverter Graph (MIG), a structure consisting of three majority nodes and regular or complemented edges. A new Boolean algebra and five primitive transformations provides a complete axiomatic system which can explore the entire MIG space. This allows MIGs to be optimized in a systematic way in terms of its size, depth or switching activity, leading to superior performance compared to the current state-of-the-art.

Advantages

The key advantage of the MIG representation and optimization is that out-performs the current state-of-the-art academic or commercial tools for digital circuit analysis.

As MIGs are a superset the more well-known And-Inverter Graph (AIG), they are able to take advantage of standard benchmark suites (for example, MCNC). MIG optimization decreases the number of logic levels by 18% on average, compared to AIG optimization run on a popular academic synthesis tool (ABC).

In standard optimization-mapping circuit synthesis flow, MIG optimization enables a reduction in the estimated delay, area and power metrics by 22%, 14% and 11%, respectively, on average before physical design, compared to academic or commercial synthesis flows.

Applications

- Electronic Design Automation (EDA)
- Superconducting electronics
- Digital circuit design flow
- Nanotechnologies